A 90W S-band High Power Amplifier for Broadband Wireless Applications

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***Abstract* — This paper describes a successfully developed 90W high power amplifier with the wide band range in S-band. The power amplifier consists of two 50W GaAs FET chips and small 180degrees coupler transmission line circuit that was developed in an external matching network. The wide band performance was achieved by the 180degrees coupler transmission line circuit and the multi-stage internal circuit. The power amplifier delivered an output power of 90W in the frequency range of 2.9 to 3.3GHz. To our knowledge, this is the highest power and frequency range ever reported in S-band. A low 3rd-order intermodulation distortion (IM3) of less than -30 dBc was also achieved at a 10 dB back-off point from saturation power in the frequency range of 2.9 to 3.4GHz. The developed power amplifier is suitable for the base station in broadband wireless access in the S-band.**

INTRODUCTION

High output power and carrier frequencies increasing are required for radar, high-capacity data transmission and internet in S-band wireless systems [1-2]. In particular, wide frequency range operation and low distortion performance are strongly demanded for realizing these systems. At present, for L-band cellular base station application, over 100W GaAs FETs have been reported [3-6]. The S-band systems use the bandwidth of several times larger than that of L-band base station. It is also essential to reduce the size and cost.

In this work, to realize the highest output power amplifier with a wide band range in S-Band, we have employed a double doped InGaAs/AlGaAs FET and also a wide band 180degrees coupler transmission line circuit designed for push-pull configuration.

FET STRUCTURE AND PERFORMANCES

We employed power double doped InGaAs/AlGaAs FET with 0.9μm-length WSi gate [5]. To obtain both high gate-to-drain breakdown voltage (BV_{gd}) and low ohmic contact resistance, a wide-recess structure was employed. The wafer was thinned to 40μm. The fabricated power FET exhibited a maximum drain current (I_{max}) of 450 mA/mm, a threshold voltage of –0.7 V and a transconductance was 300mS/mm. The BV_{gd} was over 35 V.

Fig.1 shows photograph of a developed 50W FET chip. The unit gate width and total gate width are 680μm and 150mm, respectively. To realize output power of 90W, the two 50W FET chips were used.

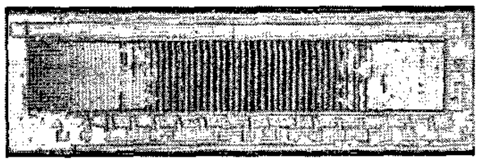

Fig.1. Photograph of a 50W FET chip.

Fig.2 shows the internal circuit network in a package. The input matching circuit consists of a LC low pass filter circuit and a transmission line circuit on an Al_2O_3 substrate. A load impedance is very low as 1Ω. Therefore, in order to reduce size of the output circuit, we employed a high εr constant substrate. The output matching impedance was obtained by a load pull measurement.

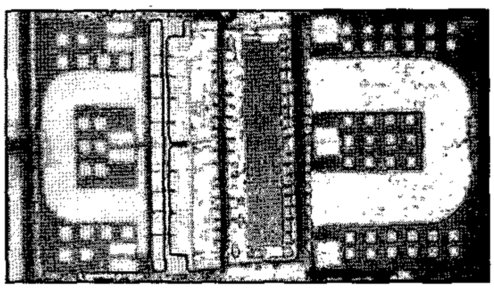

Fig. 2. Side-view of internal matching network in a package.

Fig.3 shows the top view of the two 50W FETs with the internal circuit network in a package. The feed-through impedance of the package was designed to be around 25Ω. The package size is 17 ~34mm^2.

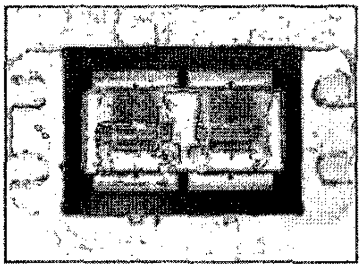

Fig. 3 Internal view of the two 50W FETs with a package.

EXTERNAL CIRCUIT DESIGN

In order to transform feed-through impedance, an external circuit was designed. The external circuit consists of the quarter wave length transformer and the 180degrees coupler transmission line circuit. Fig.4 shows equivalent circuit of the external circuit. The feed-through impedance of 25Ω is transformed by the quarter wave length transformer (S1). The transmission line length S2 and S3 are zero and half of wave length, respectively. The size reduction of circuit can be achieved by this method. Finally, the impedance of Zc (25Ω) is matched to Zt (50Ω) by the quarter wave length transformer (S4). This 180degrees coupler transmission line circuit is very simple to obtain the push-pull operation, compared to a multi-layer balun that is difficult to fabricate [1,5,7]. The EM simulation was performed for layout of the circuit. This 180degrees coupler transmission line circuit including DC bias circuit is formed on a substrate of εr=2.2. The target bandwidth is 2.9-3.4GHz. The design center frequency is 3.2GHz.

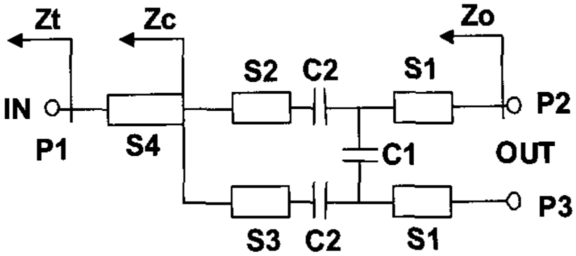

Fig. 4 Equivalent circuit of the external circuit.

Fig.5 shows the measured amplitude and phase imbalance of the circuit. In the target bandwidth, maximum amplitude and phase imbalance less than 1dB and 30degrees were obtained. At 3.2GHz, the maximum amplitude and phase imbalance were 0.6dB and 0degree, respectively.

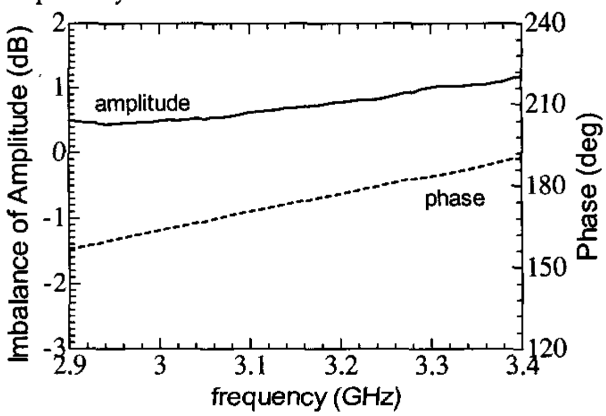

Fig. 5 Measured amplitude and phase imbalance of the 180degrees coupler transmission line circuit.

Fig.6 shows the complete amplifier circuit. The DC block capacitors were assembled in the circuit.

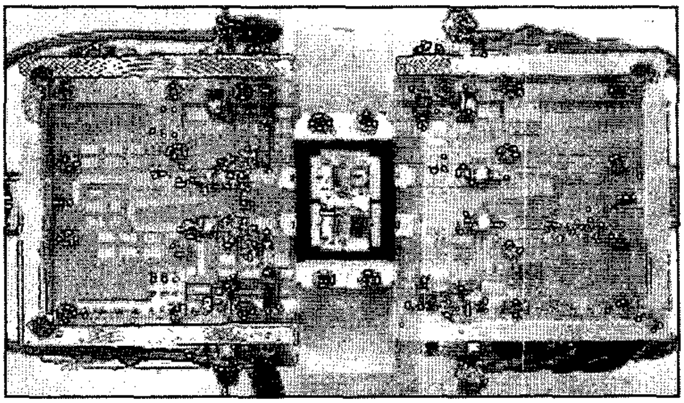

Fig. 6 Photograph of the developed S-band power amplifier.

The power amplifier size is small as 5 ~14cm^2. The package was connected with the plated-heat-sink to reduce the rise of a temperature.

RF PERFORMANCES

The measured small signal gain is shown in Fig.7. The power amplifier exhibited the small signal gain of over 9dB in the frequency range of 2.9 to 3.3GHz at a drain-source voltage (V_d) of 13V with drain-source current (I_d) of 3A.

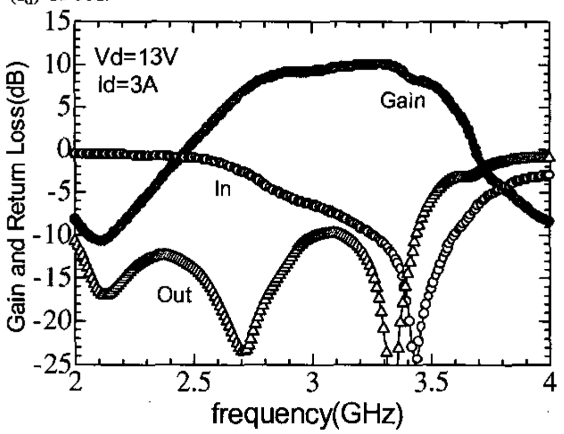

Fig. 7 Measure small signal gain characteristics.

Fig.8 shows the output power characteristics. When the power amplifier was tuned for the maximum output power at 3.2GHz, it exhibited a saturation output power (P_{sat}) of 49.7dBm (93W) with a linear gain of 9.8dB, a maximum power-added efficiency (PAE) of 36% and a maximum drain efficiency of 44% at V_d of 13V with I_d of 3A.

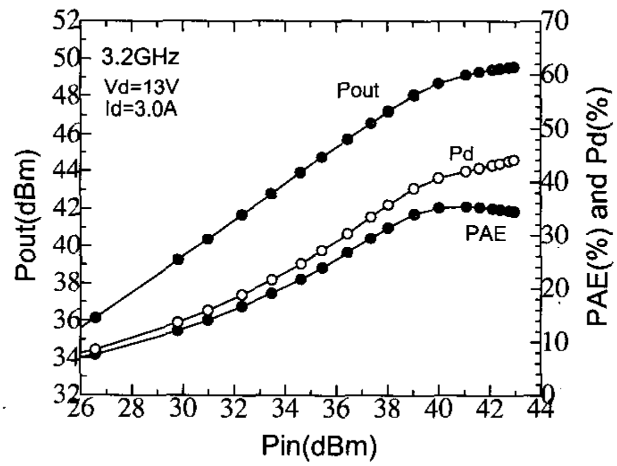

Fig. 8 Output power, power-added efficiency and drain efficiency versus input power at 3.2GHz.

To the best of our knowledge, this P_{sat} of 93W is the highest value ever reported among the power amplifier operating in over 3GHz-band [1,8-9]. Fig.9 and Fig.10 show the frequency response of output power and PAE. The power amplifier showed the output power of 90W and the PAE of 30% in the frequency range of 2.9 to 3.3GHz. The excellent frequency response across 400MHz bandwidth was achieved in the S-band.

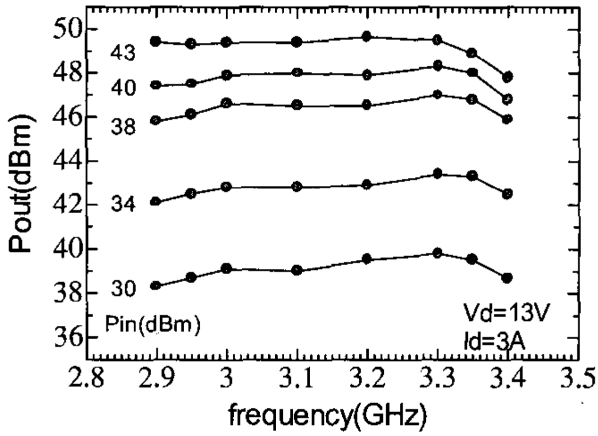

Fig. 9 Frequency response of output power.

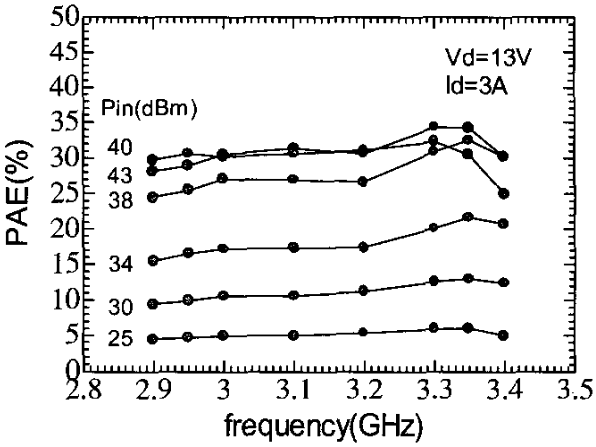

Fig. 10 Frequency response of PAE.

The frequency response of IM3 with two CW signals of 1MHz carrier spacing is shown Fig.11. The power amplifier exhibited the low IM3 characteristics of less than –30dBc at a 10 dB back-off point from total saturation power in the frequency range of 2.9 to 3.4GHz at V_d of 12V with I_d of 3A. It is notable that these high output power and low distortion characteristics with wide bandwidth was obtained at the low I_d.

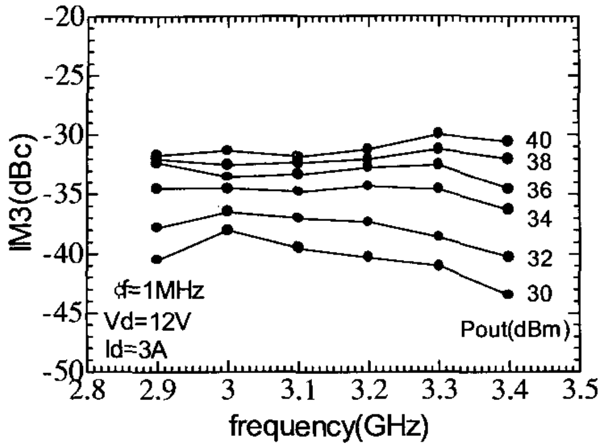

Fig. 11 Frequency response of IM3.

Fig.12 shows the output power versus bandwidth for reported S-band high-power FETs [1,8-9]. The developed high power amplifier showed the combination of the highest output power and wide bandwidth.

These results suggest that the developed power amplifier is suitable for broadband wireless applications, which require both high output power operation and low distortion characteristics in the S-band.

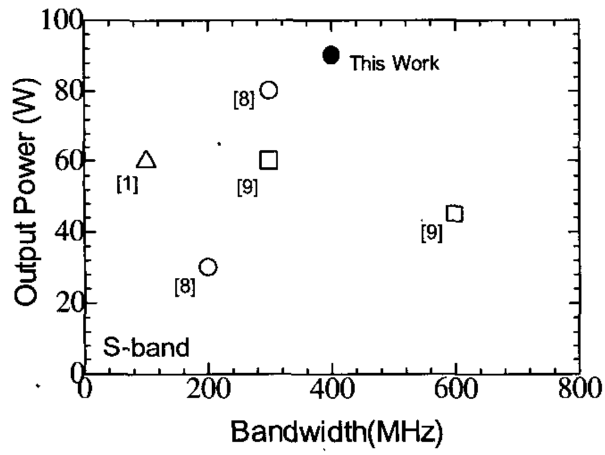

Fig. 12 Output power versus bandwidth of the developed power amplifier in comparison with published S-band power FETs.

CONCLUDION

A 3GHz 90W GaAs wide band Power amplifier has been developed. At 3.2GHz, The amplifier exhibited the highest output power of 49.7dBm (93W) with a linear gain of 9.8dB, a maximum PAE of 36% and a maximum drain efficiency of 44%. The power amplifier also showed output power of 90W and PAE of 30% with low IM3 of –30dBc in the fréquency range of 2.9 to 3.3GHz. It is notable that these high output power and low distortion characteristics with wide bandwidth was obtained at the low I_d. The developed power amplifier is promising as a wide band high power amplifier for the S-band broadband wireless applications.

ACKNOWLEDGEMENT

The authors would like to thank K.Ishikura and S.Kainuma for their helpful discussion. They also thank A.Tanaka, M.Kuzuhara and M.Mizuta for their encouragement throughout this work.

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